Accelerator Department Brookhaven National Laboratory Associated Universities, Inc. Computerized Accelerator Operating System Hardware Note: <u>D2RR-A</u>

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Function - The function of the Remote Receiver (RR) is to accept a standard Datacon2 serial, phase-encoded, bipolar pulse train^{1,2} and convert it to a number of TTL signals suitable for transmission to up to 64 device cards contained in one or more Datacon2 crates³. The RR is designed to minimize the overhead of address decoding and data formatting etc. on individual device cards, consistent with a TTL serial transmission scheme within the crate utilized to minimize the inter-card wiring. Return of data to the Datacon2 Central is similarly controlled and formatted onto the line by the RR.

Operation - Concurrent with the reception of the bipolar pulse train, the RR generates three TTL serial pulse trains containing various convenient portions of the received pulse train together with a 32 pulse RECEIVE clock suitable for shifting data into registers on the individual device cards. The RR also generates a number of signals which are static from completion of the input pulse train until the beginning of another received train. These signals represent the S/R bit and partially decoded versions of the low order 6 Datacon2 address bits. The low order 6 bits are divided into two groups, each of 3 bits decoded to 8 lines. The remaining 2 high order address bits are decoded by the RR to select a group of 64 addresses to which the RR can respond.

Upon completion of the bipolar pulse train, the RR checks the parity of the transmission and the condition of the high order address bits. If correct parity is verified and this RR is selected, the RR delays 6 µs to allow multiplexers and amplifiers to settle in the device cards and then generates a pulse called ACCEPT. This pulse initiates operation in any selected device card. When the device card has completed its operational cycle and has data to be returned to the central it pulses a line called REPLY whereupon the RR issues a 32 pulse load clock train suitable for clocking data to the RR in one or both of two data fields dependent upon the properties of the individual device. This data is formatted to the bipolar train and transmitted to the central by the RR concluding the cycle.

System Interface

HIGH=TRUE=1

EXM

EXL

These signals are used to define which group of 64 datacon channels a particular RR will correspond to. It should be noted that more than one RR may have the same EXM, EXL connections.

Address (Octal)		N=0, 400, 10	N=0, 400, 1000, 1400		
		EXM	EXL		
N+	0 - 77	0	0		
N+	100 - 177	0	1		
N+	200 - 277	1	0		
N+	300 - 377	1	1		
SET	/READ	SET/READ = LO	OW = TRUE		
		READ = HIGH =	= FALSE		

This signal is static from ACCEPT - $6~\mu s$ until the start of a new Datacon transmission.

TRUE = accept transmitted data

FALSE = reply only requested

Data Pulse Trains

ALL

TRUE = 1 = HIGH

This is a 32 bit pulse train containing the full S/R A7 - A0, M15 - M0, C6 - C0 sequence. Note that the 8 bit address field is available within this train and can be used, for instance, in controlling some multi-address devices. The rightmost n bits of the data can be obtained by shifting this train into an n bit register and allowing 32-n bits to fall off the end.

S/R + ADDRESS

TRUE = 1 = HIGH

This line carried the S/R bit and A7 through A0 address bits. Thus,

a 9 bit register with this line as input and clocked by the clock would shift through 23 bits of garbage (probably logical 0) and, upon completion of the clock train, would contain the above designated bits.

MAGNITUDE

TRUE = 1 = HIGH

This line allows transmission of the magnitude field M15 through M0 as the last 16 bits associated with the clock.

ACCEPT

A 1 μs negative going pulse which occurs 6 μs after the last RECEIVE clock pulse.

REPLY

This is a negative going pulse which must be generated by a device card having data to be returned to the RR. The device card must generate REPLY, if required, within 250 μs of ACCEPT.

CLOCK

This is a 32 bit positive going pulse train of $1/2~\mu s$ pulses spaced $3/2~\mu s$ apart, generated by the RR during transmission by the central and used to clock data into suitable registers during the receive part of the datacon sequence. Clock timing is such that data should be strobed into the device card by the leading edge of the clock pulse. If the reply line is pulsed, its trailing edge will cause an additional 32 pulses to be generated on the clock line. The reply group logic is designed to expect data to change on the falling edge of this second clock pulse train.

REPLY DATA

Reply data is organized as 2 groups of 16 bits. Since two 16 bit data fields are returned to the RR by means of 32 clocks, the RR samples Reply Group I line for the first 16 clocks and Reply Group II for the balance.

REPLY GROUP I

TRUE = 1 = LOW

Returns data in field R15 - R0 of the Datacon2 reply transmission. R15 is sent first.

REPLY GROUP II

TRUE = 1 - LOW

Returns data in field S15 - S0 of the Datacon2 reply transmission. S15 is sent first.

DATACON INPUT

A serial coded pulse train from a datacon central

COMPUTER INTERFACE

This unit acts as a translator and does not have a computer interface specification.

lines.

SIGNAL SPECIFICATIONS

Flow

In

In

Out

Out

Out

Out

Out

Out

Signal

MSHO-7

LSH0-7

EXM

EXL

S/R

ALL

S/R + Address

Magnitude

Accept

In	Reply	Expected driver is standard open collector TTL (Fan out of 10). There are 8 input lines in OR configuration. (each load is 750 Ω @ +5).
In	Reply Group I	As above
In	Reply Group II	As above
	Clock	TTL Levels Fan out of 30 (7437) on each of four outpu lines.
POWER SUPI	PLY REQUIREMENTS	
Remote Red	ceiver	Dwg. D09E476-3 Rev. A-F
+15 at	120 mA	200 us cycle rate
-15 at	300 mA	
+ 5 at	800 mA	
+ 5 at	950 mA	Rev. G
-15 at	300 mA	
Acknowleds	gments	
The :	functional design of	the remote receiver was generated during
discussion	ns between B. Culwic	k, R. Frankel, G. Smith and I. Weitman. The
logic was	designed by R. Fran	kel and the prototype built by R. Scheetz.

Description

TTL Levels Fan out of 10 (7442)

11 11 11 11

Fan out of 30 (7437) on each of four output

Jumper to Gnd or OC

As above

As above

As above

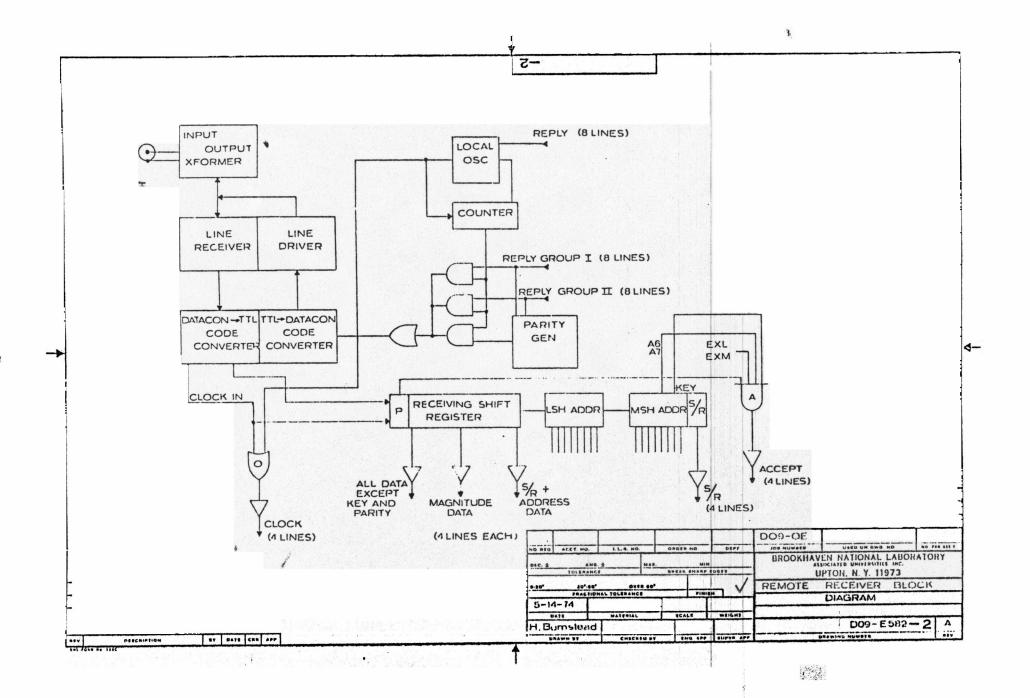
As above

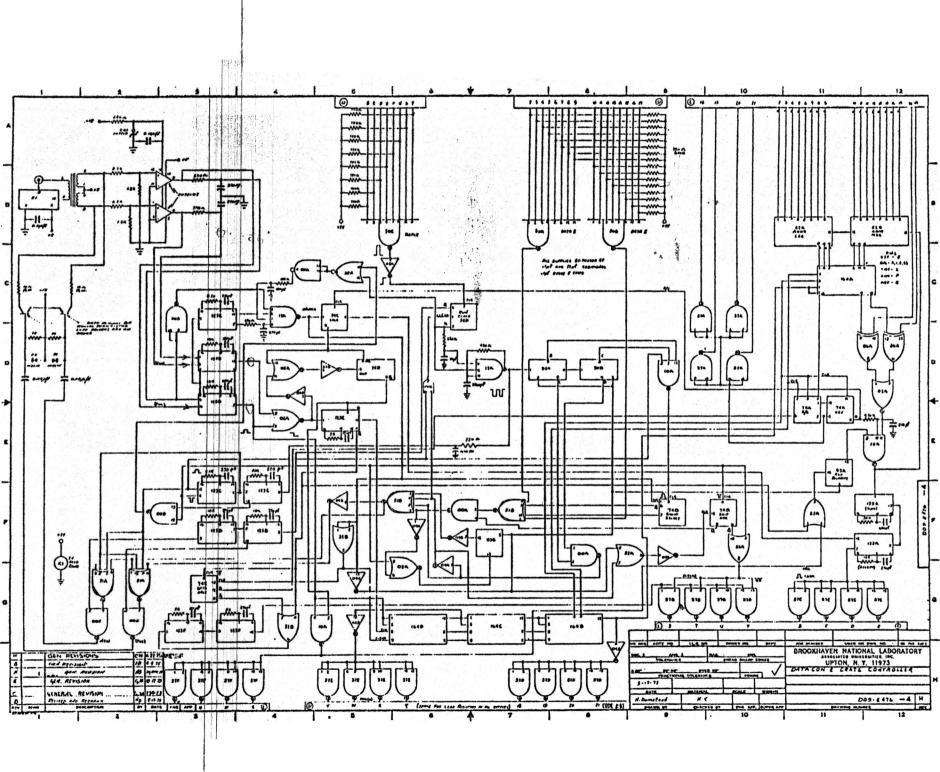
Pin Connections Remote Receiver

Connector	Pin	Signal	Addresses	Connector	<u>Pin</u>	Signal	Addresses
(B) Lower	1	Gnd			P	+157	
_ /	2	LSH ADDR=Ø	A11		R	+12(not u	sed except li
	3 .	ADDR=1	11			**	· cards)
	4	=2	n		S	Clock	0 - 17
	5	=3	**		T		20 - 37
	6	=4	***		U	Popular in the Popula	40 - 57
	7	=5	11		V		60 - 77
	8	=6	11		W	A11	40 - 57
	9	=7	11		X		60 - 77
	10	MSH ADDR=Ø	11		Y	Spare	
	11	ADDR=1	11		Z	Gnd	
	12	=2	ti				
	13	=3	11				
	14	=4	11				
	15	=5	***				
	16	=6	••				
	17	=7	Ħ				
	18	R/S	0 - 17				
	19		20 - 37				2/389
	20		40 - 57				
	21		60 - 77				
	22	Gnd					
	A	Gnd					
	В	Accept	0 - 17				
	C		20 - 27				
	D		40 - 57				
	E		60 - 77				
	F	All	0 - 17				
	H	*	20 - 37				
	J	+5V				note receiver	
	K	Spare		2 BNC	coax conr	nectors in par	allel
	L	-1 5V					
	М	EXM (1 or 0	5)				

Pin Connections Remote Receiver

Connector	<u>Pin</u>	Signal	Addresses
(A) Upper	1	Gnd	,
	2	Data Grp I	0 - 7
	3		10 - 17
	4		20 - 27
	5		30 - 37
	6		40 - 47
	7-		50 - 57
	8		60 - 67
	9		70 - 77
	10	Data Grp II	0 - 7
	11		10 - 17
	12		20 - 27
	13		30 - 37
	14		40 - 47
	15		50 - 57
	16		60 - 67
	17		70 - 77
	18	R/S + ADDR	0 - 17
	19		20 - 37
	20		40 - 57
	21		60 - 77
	22	Gnd	
	٧	Magnitude	0 - 17
	W		20 - 37
	X		40 - 57
	Y	•	60 - 77
	В	Reply	0 - 7
	C		10 - 17
	D		20 - 27
	E		30 - 37
	F		40 - 47
	H		50 - 57
	S		60 - 67
	T		70 - 77





References

- 1) EP & S Technical Note No. 50, DATACON Serial Transmission System for the PDD-11, B. B. Culwick, July 28, 1972.
- 2) EP & S Technical Note No. 58, Signal Specifications and Transceiver Operation for Datacon II System, V. J. Kovarik, March 14, 1973.
- 3) D28-1LE-741 Bucket for 10" x 10" Printed Circuit Board.